WIDE BAND, DUAL-GATE GaAs F.E.T. OUTPUT LIMITERS

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ABSTRACT

The use of dual-gate, GaAs FET devices as lower power output limiters in S- and X-Band is presented. Device characteristics, circuit design and advantages including a sharper saturation knee, small signal suppression, low loss and wide bandwidth performance are discussed.

Introduction

Previous work[1] has demonstrated the suitability of dual-gate FET's for limiting applications. The device offers several potential advantages over diode type limiters and single gate FET's operating in the saturated mode which include a sharper "knee", (defined here as the change in output power from the -1 dB compression point to the saturated level), lower saturated output powers for a given device physical size, and some measure of controllability of the saturated output level through simple DC bias level modification. Results from two wave guide bandwidth output limiters in S- and X-bands are presented here.

Device Characteristics

The devices used for this effort are in-house developed devices utilizing ion-implanted substrate material, gold based metalization systems, and 0.5 micron gate widths. Gate lengths are 250 microns. Gate 1 to gate 2 spacing is 2.0 microns and drain to source spacing is 6.5 microns. The device is designated as an M-111 and has been evaluated through 20 GHz. The devices exhibit a very flat $|S_{21}$ of about 6 dB over the 2 to 18 GHz frequency range and appear to be quite suitable for wide-band limiter applications.

Devices were measured in both a three port and two port configuration. The three port configuration was explored to provide information on the gate-to-gate transfer characteristics as well as provide full 3X3 S-parameter characterization. Gate and drain S-parameters for a typical M-111 device are plotted in Figure 1A. Figure 1B presents a table with the magnitude of the other six S-parameters listed for three frequencies. It was determined that for purposes of simplicity and efficiency two port data (with the second gate terminated in a DC and RF short) could be taken to evaluate new wafers. It is felt that this approach is justified since gate-to-gate S-parameters (S_{12} and S_{21}) appeared to be consistent from device to device and wafer to wafer. Also second gate characteristics (S_{22}, S_{23} and S_{32}) are reasonable similar to first gate ones. Additionally, in the limiter applications, second gate termination was less critical than either first gate or drain matching. Other applications requiring RF signals on all three ports, such as mixers, will require more rigorous evaluation.

Matching network design proceeded based on an average of S-parameter data taken for the wafer of interest at the anticipated bias level for the saturated output power desired.

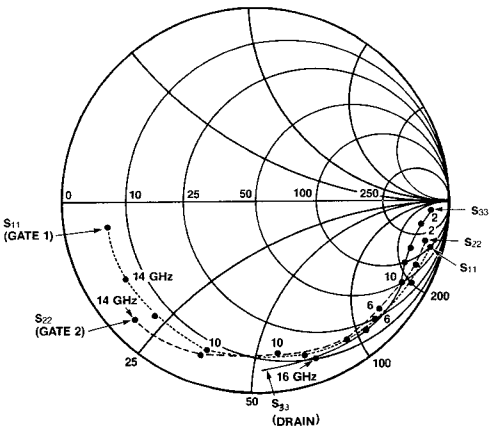

FIGURE 1A
GATE AND DRAIN CHARACTERISTICS FOR TYPICAL M-111 DUAL GATE DEVICE

	G_1–G_2		G_1–D		G_2–D	
FREQ	$\|S_{12}\|$	$\|S_{21}\|$	$\|S_{13}\|$	$\|S_{31}\|$	$\|S_{23}\|$	$\|S_{32}\|$
2 GHz	02	02	01	25	05	13
6 GHz	07	06	.02	18	12	12
12 GHz	.12	13	.09	15	25	15

FIGURE 1B
MAGNITUDES OF INTERPORT S-PARAMETERS FOR TYPICAL M-111 DUAL GATE DEVICE

[1]Mawhinney, D. D. and Rosen, A. , Final Report on FET Discriminators., NRL Contract,N00039-76-C-0280, 14 December 1976

Circuit Design

Balanced circuit designs utilized in the limiters are developed from single-ended test circuits used to evaluate matching circuits and device performance characteristics over the frequency ranges of interest. Single ended circuits are comprised of an output conjugate matching circuit to provide flat output power, the device with its associated parasitic inductances and capacitances, and an input circuit with all gain compensation to provide flat small signal gain response. Signal input is applied to gate one. Output is taken from the drain as shown in Figure 2.

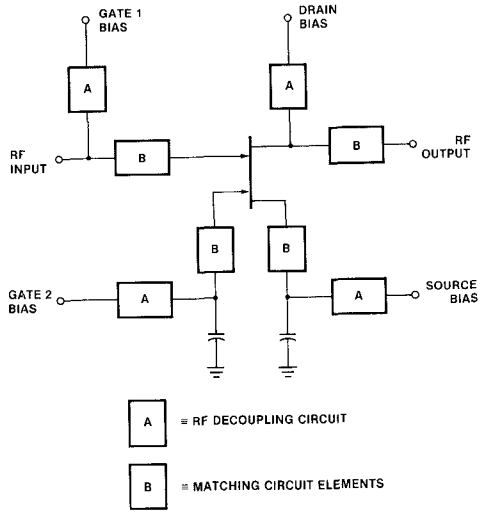

FIGURE 2 BLOCK REPRESENTATION OF SINGLE ENDED DUAL-GATE FET LIMITING CIRCUIT

Matching circuits were designed with the aid of a commercially available computerized synthesis program and an in-house analysis program. All matching circuit elements with the exception of fine tuning shunt capacitance elements are realized in lumped element form. The gate and drain matching circuits are four element networks each with two high-pass elements.

Gate two bias level can be varied allowing the saturated output power level to change. Unfortunately, it appears that a small signal gain decrease accompanies the decrease in output power when the saturated power is varied in this manner. Also, if the power is changed more than a few dB the quality of the saturation "knee" is impaired and can only be corrected partially by readjustment of first gate and drain voltages.

Performance

Table I summarizes some of the salient performance levels for the limiters developed during this program. Output power is setable over a 5 to 6 dB range but small signal gain varies over a wider range than this. The limiters do exhibit small signal suppression which is a desirable characteristic for a large number of microwave system applications.

TABLE I

BALANCED LIMITER MODULE PERFORMANCE SUMMARY

FREQUENCY RANGE	2 – 4 GHz	8 – 12 4 GHz
SATURATED POWER RANGE SETTABLE	+1 to +7 dBm	+3 to +8 dBm
SATURATED POWER FLATNESS vs FREQUENCY	±0 75 dB	±1 0 dB
SMALL SIGNAL GAIN (FOR ABOVE P_{SAT} RANGE)	−6 to +5 dB	−8 to +3 dB
SMALL SIGNAL GAIN FLATNESS (vs FREQUENCY)	±0 6 dB	±0 6 dB
RF INPUT POWER	+20 dBm MAX	+20 dBm MAX
HARMONICS	−12 dBc TYPICAL	−12 dBc TYPICAL
SMALL SIGNAL SUPPRESSION	4 dB TYPICAL	4 dB TYPICAL

Typical pulse response for a limiting amplifier is shown in Figure 3. The combination of limiter and amplifier exhibits no pulse overshoot and has a well behaved pulse response. Recovery time is about 25 n Sec. Pulse stretching is about 6 ns.

Compression characteristics for three frequencies in each of the two bands are shown in Figure 4A and 4B. The change in output power from the -1 dB gain compression point to the saturated output power level is typically less than 2 dB. One effect of the sharper knee region is to increase the available dynamic range of the limiting amplifier in which the module is used by lowering the input power point at which decompression begins for a given small signal gain amplifier. Small signal gain level shifts with temperature changes appear to be at the same level as single gate gain block stages (-.012 dB/ ^{o}C). Stability of the saturated output power over temperature appears to be slightly better than this. Typical variations are on the order of .01 dB/^{o}C although different wafers have different sensitivities. Temperature performance of the output limiting module is important since it sets the overall temperature performance for the limiting amplifier when the amplifier is in saturation.

Conclusion

The dual-gate GaAs FET has been shown to be a viable device for use in wideband output limiter circuits. Low saturated output power levels with low associated small signal insertion losses have been demonstrated. Excellent pulse response and compression characteristics make these limiters ideal for integration with amplifiers to provide attractive limiting amplifier blocks for system design.

Acknowledgments

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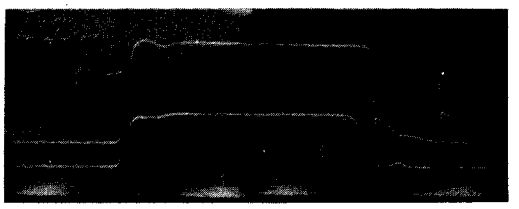

FIGURE 3

LIMITING AMPLIFIER PULSE RESPONSE.
RF FREQUENCY 10 GHz, 100 nS PULSE WIDTH
HORIZONTAL DISPLAY: 10 nS PER DIVISION

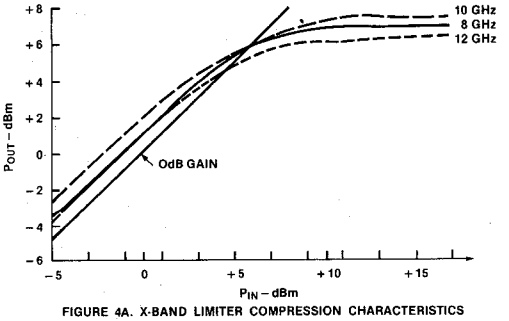

FIGURE 4A. X-BAND LIMITER COMPRESSION CHARACTERISTICS

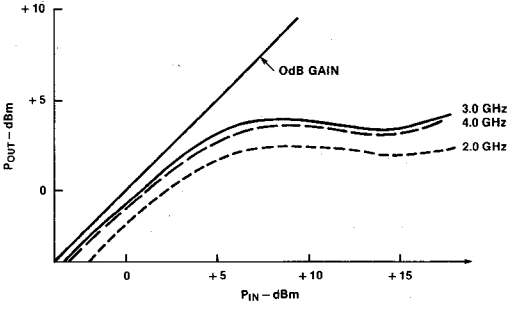

FIGURE 4B. S-BAND LIMITER COMPRESSION CHARACTERISTICS